

This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images,
please do not report the images to the
Image Problem Mailbox.

Amendments to the Claims

1. (Currently Amended) ~~An electric or electronic~~ A circuit arrangement (100) for protecting at least a chip arrangement (200), ~~for example, at least a (semiconductor) chip arrangement, particularly at least a controller chip arrangement for a chip card or smart card, from manipulation and/or abuse, characterized by comprising:~~

at least one, ~~particularly~~ optosensitive detector unit (10), comprising at least one bipolar transistor, whose output voltage (V_{out}) is a measure of the incidence of light (Li) on the detector unit (10), and

at least one comparator unit (20) preceded by the detector unit (10) provided for comparing the output voltage (V_{out}) of the detector unit (10) with a reference voltage (V_{ref}), wherein the data and/or functions of the chip arrangement (200) to be protected can be temporarily or permanently obstructed and/or erased (L) and/or blocked (S) and/or interrupted in the case of a failure message occurring during comparison of the output voltage (V_{out}) of the detector unit (10) with the reference voltage (V_{ref}).

2. (Currently Amended) A circuit arrangement (100) as claimed in claim 1, characterized in that the detector unit (10) is arranged

~~underneath the surface of the chip arrangement (200), particularly underneath at~~ least an oxide layer of the chip arrangement (200), and/or

substantially in the plane of the data and/or functions to be protected.

3. (Cancelled).

4. (Currently Amended) A circuit arrangement (100) as claimed in claim 3 1, characterized in that the detector unit (10) is constituted by a plurality or a large number of spatially arranged bipolar transistors (12).

5. (Currently Amended) A circuit arrangement (100) as claimed in claim 3 1, characterized in that ~~the~~ an emitter (124) of the bipolar transistor (12) is connected to the input (22), provided for the output voltage (V_{out}), of the comparator unit (20).

6. (Currently Amended) A circuit arrangement (100) as claimed in claim 3 1, characterized in that ~~the~~ an emitter (124) of the bipolar transistor (12) is connected to at least a power supply voltage (V_{dd}) via at least a power supply resistor (14).

7. (Currently Amended) A circuit arrangement (100) as claimed in claim 3 1, characterized in that ~~the~~ a collector (126) of the bipolar transistor (12) is connected to ground potential via at least a reference resistor (16).

8. (Currently Amended) A circuit arrangement (100) as claimed in claim 3 1, characterized in that ~~the~~ a junction between ~~the~~ a base (122) of the bipolar transistor (12) and ~~the~~ a collector (126) of the bipolar transistor (12) is provided for absorbing the light incident on the detector unit (10).

9. (Currently Amended) A circuit arrangement (100) as claimed in claim 1, characterized in that the output voltage (V_{out}) of the detector unit (10) depends on ~~the~~ a wavelength and/or ~~the~~ an intensity of the incident light (L_i).

10. (Original) A circuit arrangement (100) as claimed in claim 1, characterized in that
at least an evaluation unit (30) is implemented and/or integrated in the comparator unit (20), or
the comparator unit (20) precedes at least an evaluation unit (30).

11. (Currently Amended) A circuit arrangement (100) as claimed in claim 10, characterized in that the evaluation unit (30) generates the failure message when the output voltage (V_{out}) of the detector unit (10) deviates from ~~the~~ a nominal range.

12. (Currently Amended) A circuit arrangement (100) as claimed in claim 1, characterized in that
the a working point of the detector unit (10) and/or
the a threshold value of the reference voltage (V_{ref}) is adjustable.

13. (Currently Amended) A circuit arrangement (100) as claimed in claim 1, characterized in that
at least a dielectric coating, ~~particularly an insulation layer and/or passivation layer~~ and/or a
further protective coating which is provided for protecting the chip arrangement (200) from
external influences ~~and preferably cannot be easily removed~~ is arranged within the chip
arrangement (200) and/or laterally to the chip arrangement (200) and/or on the chip arrangement
(200).

14. (Currently Amended) A circuit arrangement (100) as claimed in claim 13, characterized in
that the a material of the dielectric coating is epoxy resin or silicon nitrite ($SiNO_2$) or silicon
dioxide (SiO_2), or other insulating materials used in the manufacture of semiconductors.

15. (Currently Amended) A circuit arrangement (100) as claimed in claim 13, characterized in
that the a material of the dielectric coating is substantially opaque.

16. (Currently Amended) A circuit arrangement (100) as claimed in claims 1, characterized in
that the chip arrangement (200) is arranged on at least a ~~particularly~~ layered carrier substrate of a
semiconducting or insulating material.

17. (Currently Amended) A circuit arrangement (100) as claimed in claim 1, characterized in that
the circuit arrangement (100) is implemented and/or integrated in ~~at least a card, particularly in at
least a chip card or in at least a smart card.~~

18. (Currently Amended) A card, ~~particularly a chip card or smart card~~, comprising at least an ~~electric or electronic~~ the circuit arrangement (100) as claimed in claim 1.

19. (Currently Amended) A chip arrangement (200), ~~for example a (semiconductor) chip arrangement, particularly a controller chip arrangement for a chip card or smart card~~, the chip arrangement comprising

at least one, ~~preferably a plurality or a large number of~~ particularly optosensitive detector units (10) as claimed in claim 1, and

at least a combination logic unit (40) for combining the detector units (10).

20. (Original) A chip arrangement (200) as claimed in claim 19, characterized in that the combination logic unit (40) is connected to at least a control logic unit (50).

21. (Currently Amended) A chip arrangement (200) as claimed in claim 19, characterized in that the combination logic unit (40) is connected to ~~at least a particularly~~ an electrically erasable storage unit (60).

22. (Currently Amended) A chip arrangement (200) as claimed in claim 21, characterized in that the storage unit (60) is constituted by at least an EEPROM storage unit (60') (EEPROM = Electrically Erasable Programmable Read-Only Memory), and the data and/or functions of the chip arrangement (200) to be protected are erasable (L) when a failure message by means of the EEPROM storage unit (60') occurs ~~particularly~~ during comparison of the output voltage (V_{out}) of the detector unit (10) with the reference voltage (V_{ref}).

23. (Currently Amended) A chip arrangement (200) as claimed in claim 20, characterized in that the storage unit (60) is arranged between the combination logic unit (40) and the control logic unit (50), and

the access to the data and/or functions of the chip arrangement (200) to be protected can be blocked by blocking (S) the storage unit (60) when a failure message occurs particularly during comparison of the output voltage (V_{out}) of the detector unit (10) with the reference voltage (V_{ref}).

24. (Currently Amended) A chip arrangement (200) as claimed in claim 19, characterized in that the chip arrangement (200) can be permanently short-circuited via the power supply voltage (V_{dd}), ~~particularly via the power supply terminals of the chip arrangement (200).~~

25. (Currently Amended) A method of protecting ~~at least a chip arrangement (200), for example at least a (semiconductor) chip arrangement, particularly at least a controller chip arrangement for a chip card or smart card from manipulation and/or abuse,~~ characterized in that

an output voltage (V_{out}) determined by light (Li) incident on ~~the~~ a detector unit (10) is generated in ~~at least a particularly an~~ optosensitive detector unit (10), ~~particularly in at least comprising a bipolar transistor (12);~~

the output voltage (V_{out}) of the detector unit (10) is compared with a reference voltage (V_{ref}) in ~~at least~~ a comparator unit (20) preceded by the detector unit (10), and

the data and/or functions of the chip arrangement (200) to be protected are temporarily or permanently obstructed and/or erased (L) and/or blocked (S) and/or interrupted when a failure message is generated during comparison of the output voltage (V_{out}) of the detector unit (10) with the reference voltage (V_{ref}).

26. (Currently Amended) A method as claimed in claim 25, characterized in that the light incident on the detector unit (10) is substantially absorbed by means of ~~the~~ a junction between ~~the~~ a base (122) of the bipolar transistor (12) and ~~the~~ a collector (126) of the bipolar transistor (12).

27. (Currently Amended) A method as claimed in claim 25, characterized in that the failure message is triggered in the comparator unit (20) when the output voltage (V_{out}) of the detector unit (10) deviates from ~~the~~ a nominal range.

28. (Currently Amended) A method as claimed in claim 25, characterized in that the triggering of the failure message is adjusted by means of

~~the~~ a working point of the detector unit (10) and/or

~~the~~ a threshold value of the reference voltage (V_{ref}).

29. (Original) A method as claimed in claim 25, characterized in that the failure message is generated in at least

an evaluation unit (30) implemented and/or integrated in the comparator unit (20),

or

an evaluation unit (30) preceded by the comparator unit (20).

30. (Currently Amended) A method as claimed in claim 25, characterized in that ~~at least~~ a control logic unit (50) connected to ~~at least~~ a combination logic unit (40) provided for combining the detector units (10) is temporarily blocked (S) when the failure message is triggered.

31. (Currently Amended) A method as claimed in claim 25, characterized in that ~~at least~~ an electrically erasable storage unit (60) arranged between at least a combination logic unit (40) provided for combining the detector units (10) and ~~at least~~ a control logic unit (50) is permanently blocked (S) when the failure message is triggered.

32. (Original) A method as claimed in claim 31, characterized in that the control logic unit (50) is temporarily or permanently blocked (S) by means of at least a "reset" (RS).

33. (Currently Amended) A method as claimed in claim 25, characterized in that a ~~particularly~~ once-electrically programmable storage unit (60) connected to ~~at least~~ a combination logic unit (40) provided for combining the detector units (10) is permanently blocked (S) when the failure message is triggered.

34. (Currently Amended) A method as claimed in claim 33, characterized in that the power supply voltage (V_{dd}) is short-circuited by means of the storage unit (60), ~~and particularly the power supply terminals of the chip arrangement (200) are short-circuited.~~

35. (Currently Amended) A method as claimed in claim 25, characterized in that the data and/or functions to be protected are erased (L) in an EEPROM storage unit (60') (EEPROM = Electrically Erasable Programmable Read-Only Memory) connected to ~~at least~~ a combination logic unit (40) provided for combining the detector units (10) when the failure message is triggered.
